A CIRCUIT TECHNIQUE FOR HIGH SPEED LOW POWER DATA TRANSFER BUS

ABSTRACT OF THE DISCLOSURE

A high speed low power data transfer bus circuit that reduces bus power consumption by imposing a limited, controlled voltage swing on the associated data bus. In one embodiment, an inverter is coupled with a pMOS pass transistor and an nMOS discharge transistor, and the combination is coupled with a data bus. The discharge transistor and pass transistor can be programmed to provide a preselected bus operational characteristics. In another embodiment, multiple nMOS discharge transistors can be coupled to the data bus via the pass transistor, with each of the discharge transistors being selectively programmed to provide additional preselected bus operational characteristics, multiple, programmable discharge transistors, thus selectably imposing encoded and multilevel logic signals on the data bus. In another embodiment, a bidirectional data transfer bus circuit couples two data busses while imposing a limited, controlled voltage swing during the transfer. One preferred embodiment couples a first data bus and a second data bus with cross-linked inverters. Interposed between the inverters, and its associated bus, is a respective pMOS pass transistor. Also, coupled between each input node and ground, is a signal discharge transistor, preferably nMOS, which facilitates data transfer between the buses. Each of the inverters is coupled with a clocked charge/discharge circuit, preferably using a common clock signal.

JFO/vat

VAT IRV1042218.1-*-2/2/01 8:49 PM